Deciding between Flip Chip and Wire Bonding

By Thomas Tschan, Product Director, ESEC, Switzerland

Production cost, packaged device performance and overall size determine the choice between flip chip and wire bonding for IC interconnecting. Here we weigh the advantages and disadvantages of each technology – and take a look at the future of flip chip.

Driven by growing demand for smaller, faster and cheaper electronic devices, the semiconductor industry continues to push inexpensive wire bonding technology to higher and higher levels. Nevertheless, for highest I/O and highest clock speed the flip chip technology has become the technology of choice. This trend is reflected by the fact that not only the vast majority of the microprocessors, but also high end ASICs and DSPs are being assembled today using flip chip technology.

Such devices are typically assembled into singulated packages. This flip chip in package technology is experiencing very strong growth compared to direct flip chip attach on board, which, in turn, is mainly used in portable applications with minimum space availability such as in cell phones, video cameras and hand held computers. Still, the mainstream packages continue to be wire bonded – as the price advantages for devices with less than 500 I/O is significant.Therefore, the main driver for flip chip technology in high-end applications is the overall performance requirements.

Today's mainstream flip chip interconnect technology is based on tin/lead solder bumps on the chip that are connected to the bond pads on a substrate. Although generating the solder bumps on the wafer is a wafer scale operation, it is an additional cost factor after the wafer has been

fully processed. After solder bumping and reflow of the bumps (see Fig. 1), the wafer is diced. In the next assembly step, the bumped die is picked from the wafer, flipped , aligned and attached to the bond pads on the substrate using a tacky flux. The fluxing of the bumps is mainly accomplished either by dipping the lower half of the bumps into a film of flux or by screen printing the flux onto the substrate. The amount of flux being used has to be well-controlled and minimized to allow for a safe reflow. The flux has two main functions; it acts as a reducing agent as well as a temporary adhesive. After placing the flipped die onto the substrate, the package is reflowed, typically in an inline reflow oven. The electrical connections are formed during this step.

To ensure the highest reliability, the next process step consists of cleaning off any flux residues from the devices. Adding the underfill and an optional encapsulation process complete the protection of the flip chip assembly.

An underfill material is required due to the significantly different expansion coefficients of silicon and the substrate material. This process step is very lengthy because only capillary forces act on the underfill deposited along the edge of the die to suck it under the die. With increasing die size, the properties of this material are increasingly crucial for a flawless underfill – as the process time and chances of air entrapment increase with die size.

Of course, there are many additional flip chip technologies. Those include a large variety of alternative bumping materials and flip chip processes, from lead based solder to lead free solder bumps, from gold stud bumping to polymer bumps and much more. Processes can range from anisotropic adhesives or films to thermocompression bonding, as well as

from simple solder reflow to thermosonic bonding, just to mention a few examples.

The pros and cons of flip chip

In flip chip technology the interconnect length between the chip and the substrate is minimal and thus, its inductance significantly lower than the one of a gold wire in a wire bonded chip. This is why the flip chip technology is the technology of choice in high clock speed applications. Besides its superior electrical behavior, the benefit of flip chip technology is the capability of connecting all the I/Os in one single process step. Additionally, the bumps can be spread over the whole chip surface (area array). This means the I/O density on the chip can be significantly higher than with wire bondable devices. This benefit allows additional power and ground connection– further increasing electrical performance.

Today's I/O count can be a few thousand I/Os at a bump pitch of 200 µm. In a few years, the I/O count is expected to reach almost 10'000 per chip at a bump pitch of 150 µm.

In the high-end flip chip market, the mainstream process is the tin lead solder, which shows a self-aligning behavior. This amazing characteristic eases the stringent placement accuracy requirements when compared to non-self-aligning processes. Tolerances usually around 12 – 15 µm (3 sigma) can stretch to 25 – 50 µm, which ultimately contribute to higher assembly speed. Nevertheless, though even the usual tolerances are still tighter than the standard epoxy die attach requirements, this 'over definition' of placement accuracy is maintained to assure that yield loss of the expensive chips from a possible rotational misalignment is kept to an absolute minimum.

Lower performance and lower pin count devices, as used in smart cards and watches, are also notable flip chip applications. These devices have

typically less than 30 I/Os and profit from the ability of the flip chip technology to meet stringent package size and height parameters. The cost of the flip chip process is compensated here with a high-volume throughput and a simplified process flow.

While the flip chip assembly benefits high performing devices, its cost is the major challenge for main stream applications. Thus, major efforts continue to be made to reduce costs. These include:

- Deposition of the underfill prior to the chip placement, thus eliminating the time consuming underfilling process by capillary action. (No Flow underfill)
- Development of cheaper bumping technologies (i.e. screenprinting of solder, use of epoxies)
- Development of lower cost substrates

While all measures target the main issue of reducing the cost of the process, an additional issue remains, the consequences of die shrink in a flip chip package. This always requires a substrate design change, which can be a very costly proposition for high I/O count devices. In comparison, wire-bonded devices only need a simple reprogramming of the wire bonder before production can resume. All the other parts and process parameters basically remain identical to the earlier chip version.

Pros and cons of wire bonding

The difference with wire bonding is that each bond is individually produced. As the die moves through the wire bonder, the machine identifies the die and each bond, then moves to each bond location to attach the interconnect, one after another. As today's leading edge wire bonders achieve up to 14 wires per second, wire bonding remains competitive to flip chip for up to about 500 I/Os per chip (see Fig. 2 and 3).

The biggest advantage of wire bonding is its process flexibility and the sheer quantity of wire bonders in use today. As a consequence, it is a mature technology and the production process is thoroughly researched and well understood. Therefore, wire bonders are a commodity, unlike the advanced die attach platforms for flip chip bonding. In addition, the wire bonding technology is extremely flexible – changes in die size can be accommodated without noticeable additional costs. New package designs and tighter control of wire length in high frequency applications have further expanded the electrical performance range of wire bonded packages.

Looking ahead for flip chip

Future trends of flip chip technology include the following innovations:

- As the disposal of electronic components containing lead is potentially hazardous to the environment, laws in Europe and Japan will ban lead in electronic assembly in a few years. Thus the introduction of lead-free solder is forced to become a reality. Currently, there are many different lead-free solder alloys in development. Other lead free alternatives, such as gold - gold, anisotropic pastes or films and epoxied bumps are being constantly optimized to meet specific price and device performance parameters and perhaps create a replacement for lead solder processes.
- Introduction of No Flow underfill in high volume productions
- Further cost reduction by development of new substrate and bumping materials.

In summary, I fully expect the flip chip market to further split into a growing number of application-specific flip chip technologies for both high-end and low-end applications.

And the winner is...

Quickly growing market demand for flip chip is assured through the increasing need for continually smaller and higher performance chips. However, as long as the inherent flip chip disadvantages of lower design change flexibility and higher production process costs remain, it will not move much beyond established high-end and low-end applications. Wire bonding processes are well known, cost effective, highly flexible and have an enormous installed system base. This alone ensures that wire bonding will remain the main technology for interconnecting ICs for many years to come - while flip chip will continue to gain market share but will not take over the lead in interconnection technology in the near future.

(author bio)

Dr. Thomas Tschan is Product Director at ESEC (Switzerland) for the Micron product line (the advanced die attach platform for high-end flip chip and MCM applications). He earned his Ph.D. at the University of Neuchatel, Switzerland, in the field of MEMS devices. Following his studies, Dr. Tschan was the R&D director for a Silicon Valley sensor company where he was responsible for the development of micromachined accelerometers. In 1995 he joined ESEC and has held various positions in strategic Marketing and New Developments prior to become the Product Director for the Micron product line.

Figure Captions :

Fig. 1 : Solder bumps on a high I/O flip chip device

Fig. 2 : Very short wire loop as used in chip scale packages

Fig. 3 : staggered wire bonds for maximum I/O density in wire bonded devices